REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 112, second paragraph Rejections

Examiner rejected claims 6-7, 16-17, 25-26, and 29 under 35 U.S.C. § 112, second paragraph, as having insufficient antecedent basis for limitations within the claims. Appropriate corrections have been made.

35 U.S.C. § 102(b) Rejections

Examiner rejected claims 1-7, 9-17, 19-20, 31-32, and 34-35 under 35 U.S.C. § 102(b) as being anticipated over U.S. Patent 5,760,636 (hereinafter "Noble").

> To anticipate a claims, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Applicant's independent claims include limitations not disclosed nor suggested by Noble. Therefore, applicant's independent claims are not anticipated by Noble.

In particular, applicant's independent claims 1, 21 and 31 include the limitation, or limitation similar thereto, of:

> *a controller to transition, in response to the power management event, a first setting of the processor from a first performance mode to a second performance mode, including to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level,* ***the processor to remain in an active mode during the voltage level transition***. (emphasis added). (Applicant's claim 1).

As well, applicant's independent claims 11, 21 and 34 include the limitation, or limitation similar thereto, of:

> *a controller to transition the processor, in response to the power management event, the transition includes to lower the core processor clock frequency from a first frequency to a second frequency, and to lower the core processor supply voltage level from a first voltage level to a second voltage level,* ***the processor to remain in an active mode during the voltage level transition***. (emphasis added). (Applicant's claim 11).

Noble, however, does not discloses nor suggest ***the processor to remain in an active mode during the voltage level transition***, as claimed by applicant. Rather, Nobel discloses the processor remaining active during the frequency level transition:

> In accordance with one embodiment of the present invention, the transition from normal operation mode to lower power mode as well as the transition from the low power mode back to the normal operation mode both involve dynamic clock frequency adjustment in that the processor, along with the rest of the computer system, continues to execute instructions for the user throughout the transitional periods. (Nobel, col. 5, lines 36-41).

Therefore, considering applicant's independent claims include limitations that are not disclosed nor suggested by Noble applicant's independent claims are not anticipated by Noble.

Furthermore, the remaining claims that were also rejected as being anticipated by Noble, depend from one of the independent claims discussed above and therefore also include the distinguishing claim limitations. As a result, the remaining claims are also not anticipated by Noble.

CONCLUSION

Applicant respectfully submits the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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